PA-IDC

| QUERY CONTROL FORM | | | | RTIS USE ONLY | |
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| Application No. | 10/024,661 | Prepared by | ewc | Tracking Number | 05917219 |
| Examiner-GAU | Le<br>2819 | Date | 4/7/04 | Week Date | 3-08-04 |
| | | No. of queries | - 1 - | | IFW |

| JACKET | | | |
|---|---|---|---|
| a. Serial No. | f. Foreign Priority | k. Print Claim(s) | p. PTO-1449 |
| b. Applicant(s) | g. Disclaimer | l. Print Fig. | q. PTOL-85b |
| c. Continuing Data | h. Microfiche Appendix | m. Searched Column | r. Abstract |
| d. PCT | i. Title | n. PTO-270/328 | s. Sheets/Figs |
| e. Domestic Priority | j. Claims Allowed | o. PTO-892 | t. Other |

| SPECIFICATION | MESSAGE |
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| a. Page Missing | Continuing data on pg 1 sheet is |
| b. Text Continuity | not in specification. |
| c. Holes through Data | Please advise |
| d. Other Missing Text | Thank you |
| e. Illegible Text | ewc |
| f. Duplicate Text | |
| g. Brief Description | |
| h. Sequence Listing | |
| i. Appendix | |
| j. Amendments | |
| k. Other | |
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| **CLAIMS** | |
| a. Claim(s) Missing | |
| b. Improper Dependency | |
| c. Duplicate Numbers | |
| d. Incorrect Numbering | initials |
| e. Index Disagrees | **RESPONSE** |
| f. Punctuation | Corrected |
| g. Amendments | |
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| k. Other | |
| | initials 4/13/04 |

E-5 (Rev. 10/01/02)

# Programmable Multi-standard I/O Architecture for FPGAs

THIS APPLICATION IS A CON OF 09/738,508 12/18/2000
WHICH IS A DIV OF 09/224,929 12/31/1998 PAT 6,242,943

## BACKGROUND OF THE INVENTION

### Field of the Invention

The invention relates to Field Programmable gate Arrays. It relates to a configurable I/O architecture that allows user configuration of I/O modules of an FPGA.

### Prior Art

Almost all integrated circuits (IC) use I/O buffers to connect internal circuit node to other circuits external to the IC. These I/O buffers can be Input, Output or bidirectional I/O. Further, each I/O buffer is designed to meet electrical specifications dictated by industry standards such as TTL, LVTTL, LVCMOS, GTL . It is also common for circuit designers to design each I/O buffer with multiple transistors in parallel. For example, 2 -4 P-type transistors may be connected in parallel to form the pullup section of the buffer, while 2-4 N-type transistors may connected in parallel to form the pulldown section of the buffer. Designers may then decide to use some or all of the transistors as needed by the circuit application to meet performance criteria, a particular I/O standard and noise considerations.

Selection of the transistors connected into the circuit is usually done by masking options such as metal, Vias and contacts. Further, some FPGAs have used similar techniques to select one or more transistors into the I/O buffer to provide slew control. One such FPGA that performs this function is the ACT 1280 FPGA from Actel corporation. A user may configure his I/O buffer to have either fast slew or slow slew by programming an appropriate